GIGAHERTZ RATE COUNTER LOGIC AND CLOCK GENERATION USING HIGH F_T TRANSISTORS

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Summary

Gigabit-rate communications will use high speed logic systems which will use gigahertz-rate bi-stable devices for various logic functions including waveform generation. The chief requirement of such devices is the generation of square-wave and steep-rise-front voltage, current, and power functions. This paper will review the long art of bi-stable devices and will compare the features of each including considerations of speed and developed voltage. The impact of new transistors with high F_T's will be discussed, and experimental counter logic devices will be discussed which count at speeds at one gigahertz, and will include a discussion of experimental signal sources developing waveforms such as square waves, and pseudo random codes at gigahertz rates.

Description

When the bit rate of digital data approaches gigahertz rates, then the devices producing the data join the microwave device community. In general, high speed digital data utilizes a two-state type of waveform as shown in Fig. 1B and Fig. 1C as compared to the sine wave of Fig. 1A which is the basic waveform of analog devices. Due to the occurrence of time delay and rise and fall times in practical circuits, waveforms of the type shown in Fig. 1B are encountered in high speed systems and the devices used as gates and bi-stable (two-state) devices must be designed to maximize the rectangularity of the waveforms and to assure positive and non-ambiguous switching between states.

Microwave data rates are not new; in fact tunnel diode flip-flops and phase locked oscillators were designed to perform logic functions in excess of gigahertz rates more than a decade ago. However the advent of microwave transistors with F_T's well above 4 GHz and in excess of 10 GHz has made possible gates and logic elements capable of subnanosecond logic speeds. At one gigabit data rate, each bit requires one nanosecond duration time which must also include both the rise time and fall time of the waveform; using from 10% to 15% rise or fall time as a reasonable criterion, it follows that in order for logic functions to optimally occur, rise and fall times and delay times must be of the order of 150 to 200 nanoseconds which can be accomplished at the gigabit rate with high F_T transistors wherein the delay time figure of merit, τ, is related to transistor parameters such as transistor F_T and the transistor base resistance r_b and collector capacitance C_c by the relationship

$$\tau = \sqrt{\frac{r_b C_c}{F_T}}$$

For F_T's less than 10 GHz and to a minimum value of 4 GHz with optimum $r_b C_c$, logic functions and waveforms can be generated but with decreasing rectangularity. In addition to these transistor parameters, critical circuit parameters such as propagation time, characteristic impedance, dissipation, and peak-to-peak logic swing must be selected and designed to be compatible with the data rate.

In order to achieve microwave bit rates, non-saturating transistor circuits must be used. Emitter coupled logic is the fastest mode possible with transistor circuits since it relies on the transistor operating in the linear range of its characteristics, and the current-routing gate and the bi-stable flip-flop of Fig. 2 are typical of these basic circuits.

In general logic circuits of the gate and flip-flop variety are complex arrangements of individual emitter coupled logic (ECL) gates and driving, set, reset, and coupling circuits. Figures 3 and 4 show clock toggled and clocked set-reset flip-flops using ECL gates capable of operating as bi-stable circuits into the gigabit range. Fig. 4 illustrates some of the thick-film concepts employed with the flip-flop arrangement.

Figure 5 shows the high speed toggled flip-flop of Fig. 3 operated at clock speeds of 500, 750, and 1000 MHz per second. The transistor used had measured characteristics of F_T = 4 GHz, R_s = 75 ohms, and C_c = 1 pf. Rectangular waveforms were maintained to almost 1 GHz and clean discrete counting was observed at 1 GHz. The F_T was the lowest which permitted accurate counting at 1-GHz. With newly available transistors with 10 GHz, F_T's, excellent rectangularity of output waveform at 1-GHz could be achieved. Figures 6 and 7 show respectively how 1-GHz flip-flops can be connected to provide fast PRN codes; Figure 7 shows how four 250 Mbps PRN code generators can be multiplexed using 1-GHz flip-flops and gates to produce a 1-GHz PRN code. Figure 8 shows a 215 Mbps PRN code developed by the 7-flip-flop register of Fig. 6 using 1-GHz logic elements showing the excellent rectangularity of the waveforms which can be achieved.

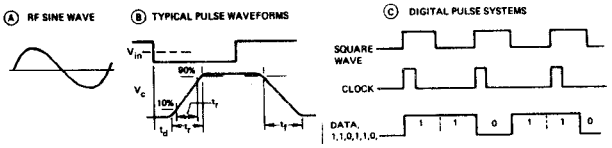


Figure 1: Typical Analog (A) and Digital (B)(C) Waveforms

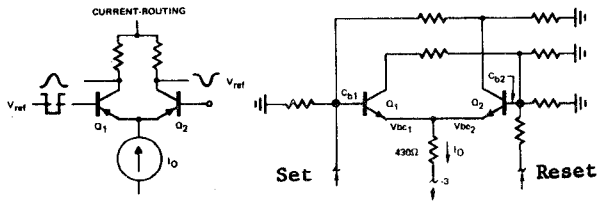


Figure 2: High Speed Emitter Coupled Current Gate (left) and Bi-Stable Circuit (right)

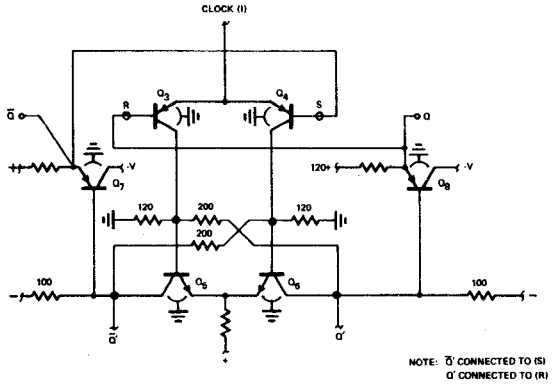


Figure 3: High Speed Toggled Flip-Flop

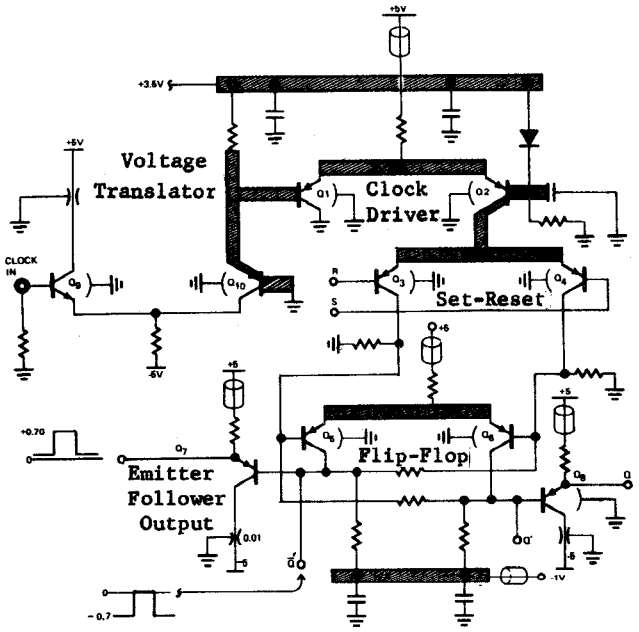


Figure 4: Gigahertz Rate Clocked Set/Reset Flip-Flop

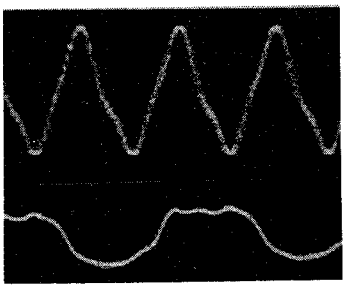
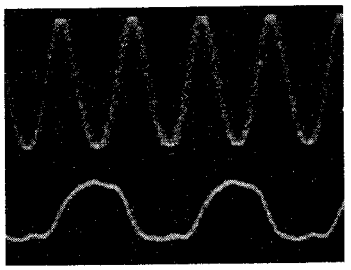
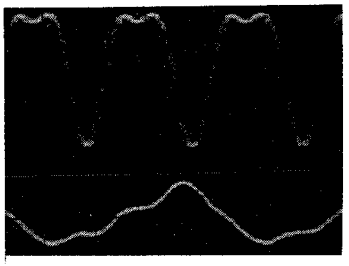


Figure 5: Waveforms of Circuit of Fig.3 Using 4 GHz F_T Transistor

Clock
1 ns/cm
Flip-Flop Output at Q
500 MHz



Clock
1 ns/cm
Flip-Flop Output at Q
750 MHz



Clock
0.5 ns/cm
Flip-Flop Output at Q
1 GHz

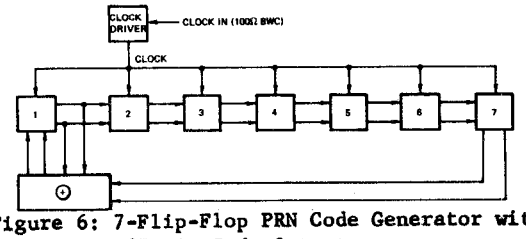


Figure 6: 7-Flip-Flop PRN Code Generator with 127 Bit Code Output

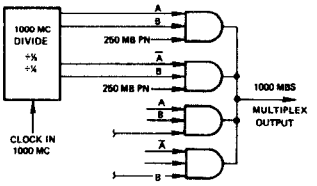


Figure 7: GHz PRN Code Multiplexed Waveform Generator

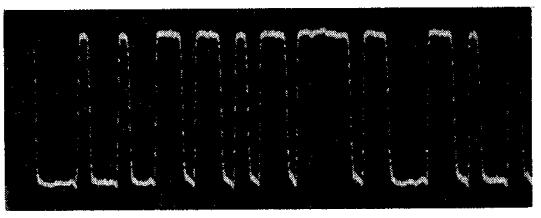


Figure 8: 215 MHz PRN Code Waveform Using 1 GHz Flip-Flops in Fig. 6 Configuration